ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device with a small layout area, having a memory cell array including a plurality of memory cells arranged in a column direction and a row direction, wherein: each of the memory cells has a source region, a drain region, a channel region disposed between the source region and the drain region, a select gate and a word gate disposed to face the channel region, and a non-volatile memory element provided between the word gate and the channel region; and a longitudinal section of the word gate has a base, a side which is perpendicular to the base, and a curved side which connects the base to the side.